Roll No. .....

24324

B. Tech 6th Semester (CSE) Examination – May, 2018

DIGITAL SYSTEM DESIGN

Paper : EE-310-F

Time : Three Hours] *[Maximum Marks : 100*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt *five* question in all, selecting *one* question from each Section. Question No. 1 is *compulsory*. All questions carry equal marks.

1. (i) Define data types and data objects. 5
   (ii) Differentiate between concurrent and sequential statement. 5
   (iii) Explain why simulation is required. 5
   (iv) What is GAL ? 5

SECTION – A

2. (a) Discuss different types of delay models used in VHDL. 15
   (b) Explain different types of operator used in VHDL. 5

3. What is overloading ? Explain different types of overloading used in VHDL with suitable examples in detail. 20

SECTION – B

4. Explain the following : 20

   (i) Procedures

   (ii) Package and Library

   (iii) Component declaration and instantation

   (iv) Generics

5. (a) Write VHDL code for 4:1 Mux using

      (i) Case Statement

      (ii) If Then Else statement 10

   (b) What is the difference between function and procedures ? Explain with the help of examples. 10

SECTION – C

6. (a) Write VHDL code for design of an Mod-10 asynchronous counter. 10

   (b) Implement the following Boolean function $F = B + CD + AE$ using :

      (i) Nand- Nand logic

      (ii) Nor-Nor logic 10

7. Write VHDL code for the following sequential circuit : 20

(i) SISO shift register

(ii) 1:16 Demux

SECTION – D

8. Write short note on : 20

(i) PEEL

(ii) FPGA

(iii) CPLD

9. (a) Implement $F(A,B,C,D) = \Sigma (2,4,6,7)$ using PAL. 10

(b) Draw and discuss in detail the architecture of simple micro computer. 10