24043

B. Tech. 3rd Semester (IT)

Examination – December, 2018

DIGITAL ELECTRONICS

Paper : EE-204-F

Time : Three Hours]   *[Maximum Marks : 100*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt *five* questions in all, selecting *one* question from each Section. Question No. 1 is *compulsory.*

1. (a) Draw and give truth table of :

    (i) Ex-or Gate

    (ii) NOR Gate

  (b) What is difference between combinational and sequential circuits ?

  (c) Draw and explain 1 bit comparator.

  (d) Write a short note on PAL. $5 \times 4 = 20$

SECTION – A

2. (a) Simplify the given expression using the Quinic. Mc Cluskey minimization technique and realize it using basic gates : **15**

$$Y(A, B, C, D) = \Sigma m\,(0, 1, 3, 7, 8, 9, 11, 15)$$

(b) What are universal gates ? Derive basic gate from any one universal gate. **5**

3. (a) Design the ckt after minimization using k-Map : **15**

$$f = \Sigma m\,(0, 1, 2, 3, 6, 7, 9, 13) + \Sigma d\,(11, 15)$$

(b) 7 bit Hamming code 1101101 is received. Check whether it is correct or not ? Correct it, if it is incorrect. **5**

SECTION – B

4. (a) Explain full adder circuit. **10**

(b) Design 16 : 1 multiplexer using 8 : 1 multiplexer. **10**

5. (a) Implement the following expression using a multiplexer : **6**

$$f = \Sigma m\,(0, 2, 4, 6)$$

(b) Explain the function of Demultiplexer in detail with its diagram. **6**

(c) Write a short note on priority encoder. **8**

SECTION – C

6. (a) Convert a JK flip flop to T fliop flop. **10**

(b) What is race around condition and how we can remove it ? **10**

7. (a) Design a 3 bit synchronous counter using JK flip flop. **10**

(b) Describe the bidirectional shift register with the help of circuit diagram. **10**

SECTION – D

8. (a) Draw primitive flow table and non primitive flow table. **10**

(b) Write a short note on hazards. **10**

9. Write short note on : **10 × 2 = 20**

(a) PLDs and CPLDs

(b) PLD and CPGA

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