B.Tech. 4th Semester (EE) F-Scheme Examination,
May–2018
DIGITAL ELECTRONICS
Paper–EE–204–F

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt **five** questions. **Question No. 1 is compulsory.** Attempt at least **one** question from each of four sections.*

1. (a) Draw and give truth table of :
   (i) EX-OR gate
   (ii) EX NOR gate.
   (b) Draw and explain 1:4 demultiplexer.
   (c) Differentiate Latch and Flip-Flop.
   (d) Differentiate between ASLC and SSLC. 4×5=20

Section–A

2. Simplify the logic function using Quin Mc Clusby method :

$$f(A, B, C, D) = \sum_m (1, 4, 8, 10, 15) + d(0, 3, 5).$$

20

3. (i) Multiply $(11011.101)_2$ by $(1001.101)_2$.

(ii) Convert $(ADB764)_{16}$ to ($)_8$.

(iii) Convert $(234.5)_{10}$ to ($)_2$.

(iv) Subtract 7 – 5 using 2's compliment.

(v) Divide $(110011.10101)_2$ by $(11001)_2$. 5×4=20

Section–B

4. Explain binary adder and subtractor. 20

5. (a) Differentiate between MUX and ENCODER with suitable examples. 10

(b) Draw bleach diagram, truth table and circuit diagram for 1-bit comparator. 10

Section–C

6. Explain bi-directional shift register. 20

7. (a) Design Mod 6 UP/Down counter using T-type flip-flop. 10

(b) Construct a D-flip flop using JK flip flop. 10

Section–D

8. (a) What is the advantages of ECL logic family ? Explain how ECL gate works. 10

   (b) Explain the R–2–R Ladder type D/A converter. 10

9. Write short notes on : 20

   (i) Structure of PLA.

   (ii) ROM and FPGA.